In the Claims:

1. (Currently Amended) A method of precharging a bank of memory cells in a semiconductor memory device, the method comprising:

receiving a command that includes an auto-precharge function to the semiconductor memory device;

initiating a timer in response to the received command; and

automatically precharging the bank responsive to the timer reaching ~~reaches~~ a predetermined value.

2. (Original) The method of Claim 1, wherein the received command is associated with data stored in a specific row of the bank, and wherein the method further comprises resetting the timer when prior to the timer reaching the predetermined value a second command is received by the semiconductor memory device that is associated with additional data stored in the specific row of the bank.

3. (Original) The method of Claim 1, wherein the received command is associated with data stored in a specific row of the bank, and wherein the method further comprises precharging the bank when prior to the timer reaching the predetermined value a second command is received by the semiconductor memory device that is associated with data stored in a different row of the bank.

4. (Original) The method of Claim 1, wherein the received command is associated with data stored in a specific row of the bank, and wherein the specific row of the bank is left open for a period of time after an operation associated with the command is completed.

5. (Original) The method of Claim 4, wherein the received command is a first read command, and wherein the method further comprises performing a first read operation in response to the first read command and performing a second read operation after completion of the first read operation using a page mode operation.

6. (Original) The method of Claim 1, the method further comprising initiating a second timer in response to the received command and storing a row address associated with the received command.

7. (Original) A semiconductor memory device, comprising:

a memory cell array arranged in rows and columns; and

a precharge control circuit having at least one timer, wherein the precharge control circuit is configured to issue a precharge control signal to the memory cell array responsive to receipt of a command that includes an auto-precharge function a predetermined time after the command is received.

8. (Original) The semiconductor memory device of Claim 7, wherein the precharge control circuit issues an auto-precharge control signal to the memory cell array responsive to the at least one timer reaching the predetermined time.

9. (Original) The semiconductor memory device of Claim 8, further comprising a storage device that stores the predetermined time.

10. (Original) The semiconductor memory device of Claim 9, wherein the semiconductor memory device further comprises a second timer that measures passage of the predetermined auto-precharge time and a row address storage register that is associated with the second timer.

11. (Original) The semiconductor memory device of Claim 7, further comprising a row decoder for decoding an externally received row address and a command decoder that activates an auto-precharge control signal in response to the input of a command having the auto-precharge function.

12. (Original) A method of precharging a bank of memory cells in a semiconductor memory device, the method comprising:

receiving at the semiconductor memory device a read command that includes an auto-precharge function;

starting a timer responsive to receiving the received read command;

performing a read operation responsive to the received read command;

delaying initiation of an auto-precharge operation called for by the auto-precharge function until the timer reaches a predetermined time.

13. (Original) A method of reading data from a semiconductor memory device, the method comprising:

receiving a read command that includes an auto-precharge function at the semiconductor memory device;

reading a first data bit from a cell in a first bank of cells in the semiconductor memory device in response to the received read command; and

using a page mode operation to read a second data bit from a second cell in the first bank of cells in the semiconductor memory device in response to a second read command.

14. (Original) The method of Claim 13, further comprising initiating a timer that measures an auto-precharge delay period in response to receiving the first read command.

15. (Original) The method of Claim 14, further comprising resetting the timer in response to the input of the second read command.

16. (Original) A semiconductor memory device comprising:

a memory cell array disposed in rows and columns;

a row decoder for decoding an externally received row address;

a command decoder for decoding externally received commands and activating an auto-precharge control signal when a decoded command includes an auto-precharge function; and

a precharge control circuit that includes at least one timer that is reset in response to the auto-precharge control signal and that initiates precharging of at least a part of the memory cell array when the at least one timer reaches a predetermined value.

17. (Original) The semiconductor memory device of Claim 16, further comprising a program register that stores timing information about when the at least part of the memory cell array is precharged.

18. (Original) The semiconductor memory device of Claim 17, wherein the precharge control circuit causes the memory cell array to be precharged when the timer reaches a value of the timing information stored in the program register.

19. (Original) The semiconductor memory device of Claim 18, wherein the program register is a mode register set.

20. (Original) The semiconductor memory device of Claim 16, wherein the memory device is a DRAM device.

21. (Original) A semiconductor memory device comprising:

a plurality of banks having a plurality of memory cells disposed in rows and columns;

a bank selector for selecting one of the banks in response to an externally received bank address;

a row selector for selecting one row of the selected bank in response to an externally received row address;

a command decoder for decoding a externally received command and activating an auto-precharge control signal when the decoded command has an auto-precharge function; and

a precharge control circuit that includes a plurality of timers corresponding to the plurality of banks, respectively,

wherein the timer corresponding to the selected bank is reset in response to auto-precharge control signal, and controls the bank to be precharged when the timer reaches a predetermined value.

22. (Original) The semiconductor memory device of Claim 21, further comprising a program register that stores timing information regarding when the selected bank is precharged.

23. (Original) The semiconductor memory device of Claim 22, wherein the precharge control circuit causes the selected bank to be precharged when the timer reaches a value of the timing information stored in the program register.

24. (Original) The semiconductor memory device of Claim 22, wherein the program register is mode register set.